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Programming Intel's 27256 EPROM

Robert Davis
Applications Engineering
Non-Volatile Memory Division
Intel Corporation

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INTRODUCTION

With the introduction of the 27256 32K byte EPROM, a new generation of high density componentized software is possible. Intel's process and product technology advances have increased EPROM memory storage capabilities from 2K bits to 256K bits. This non-volatile memory can allow the designer a more reliable, user-friendly system. Since it is produced in the 28 pin JEDEC-approved Intel universal site, the 27256 can easily be designed into existing printed circuit boards.

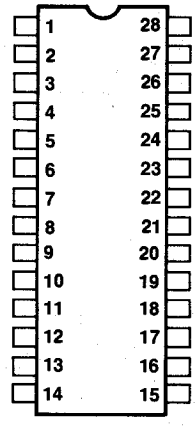
Figure 1 shows the evolution of Intel's EPROM family. The new generation 27256 brings with it improved performance and state-of-the-art reliability. The absence of $\overline{PGM}$, replaced by A14, and a lower programming voltage (12.5V) highlight the additions accompanying the 27256. Advanced technology from the 27256 will soon bring enhanced performance to lower density EPROMs, specifically the 2764A and 27128A. This document concerns programming characteristics of the 27256, concentrating on those factors which will be new to the EPROM memory designer.

THE int$_e$ligent Programming™ ALGORITHM

The int$_e$ligent Programming™ Algorithm was developed as an improved alternative to the 50 msec per byte programming techniques for Intel's 2764 and 27128 EPROMs. By taking advantage of the variable programming times required by the cells in an EPROM array, programming speed increases of 5 or 6 times have been achieved. The success of this algorithm, coupled with the long programming times which would be inherent in programming the 27256 with a 50 msec per byte algorithm, has prompted Intel to develop a new 27256 int$_e$ligent Programming Algorithm specifically tailored to the requirements of the customer.

The 27256 programming algorithm is similar to the int$_e$ligent Programming Algorithms used for Intel's 2764 and 27128 EPROMs. It is now available as a standard feature in many PROM programmers. This new programming algorithm is fast and guarantees that each cell has been programmed reliably.

27256	27128	2764	2732A	2716
V_{PP}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd	Gnd



2716	2732A	2764	27128	27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A_{14}
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 1. Intel Universal Memory Site for EPROMs

The 27256 int$_e$ligent Programming Algorithm shown in figure 2 is a feedback control loop. In examining this diagram, three distinct characteristics can be seen. First, the programming voltage has been reduced from 21 ±0.5 volts, as was required on earlier generation 2764 and 27128 EPROMs, to 12.5 ± 0.5 volts. In all cases the V_{PP} voltage should never exceed 14 volts, and a 0.1 microfarad capacitor should be placed between V_{PP} and ground to insure proper decoupling. The technology advances implemented in the 27256 allow the programming voltage to be reduced while taking advantage of the performance of the programmed cell. The second characteristic that should be noted is the maximum number of 1ms pulses which are applied throughout the closed loop programming algorithm. As shown, 25 iterations of the loop is the maximum number allowed. Intel's reliability data indicate that 25 iterations is sufficient to reliably program each of the EPROM bits in the array. The last characteristic which should be mentioned is the insertion of a byte verify after the iteration count has been maximized. This will save time by failing any device which may not verify correctly after 25 one msec pulses.

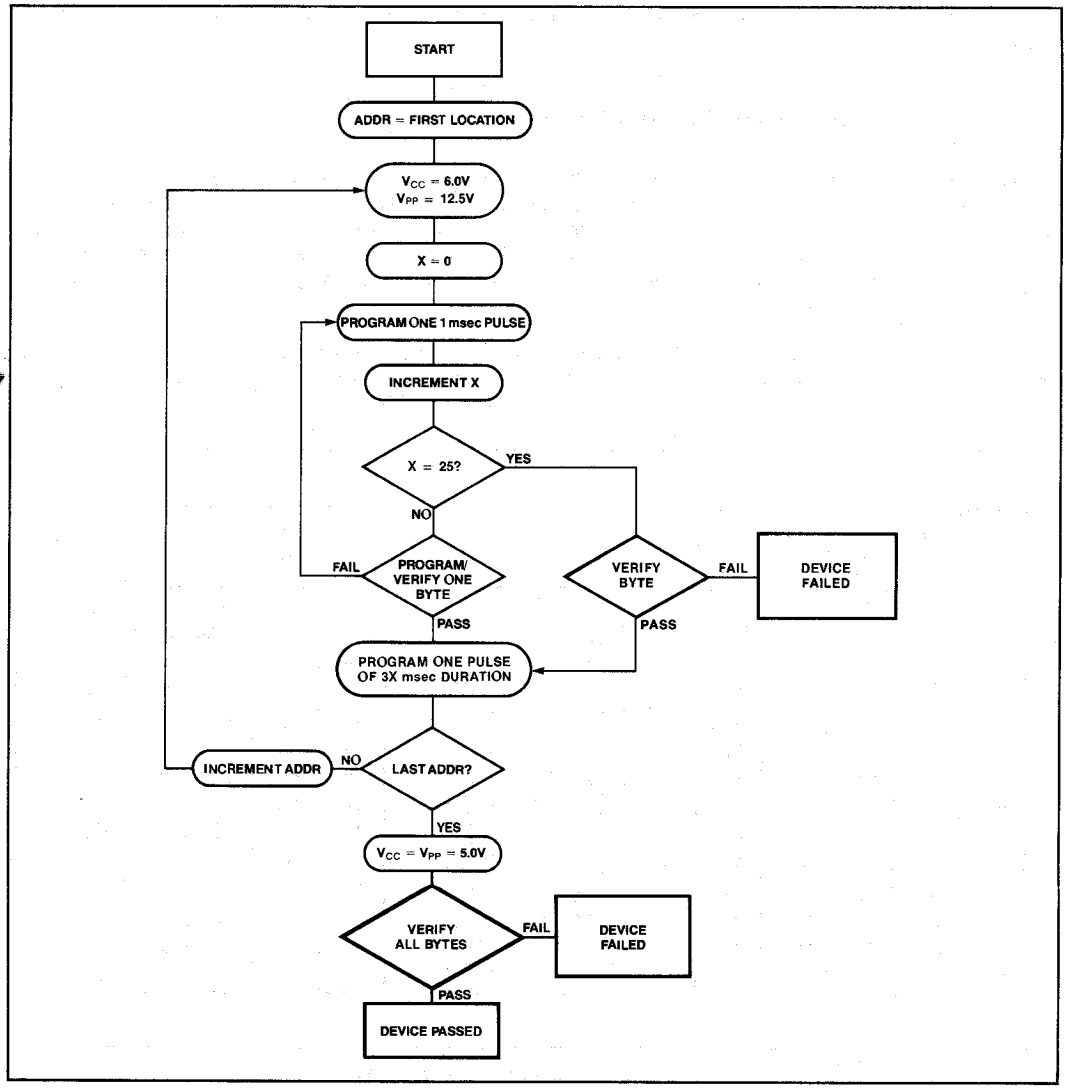
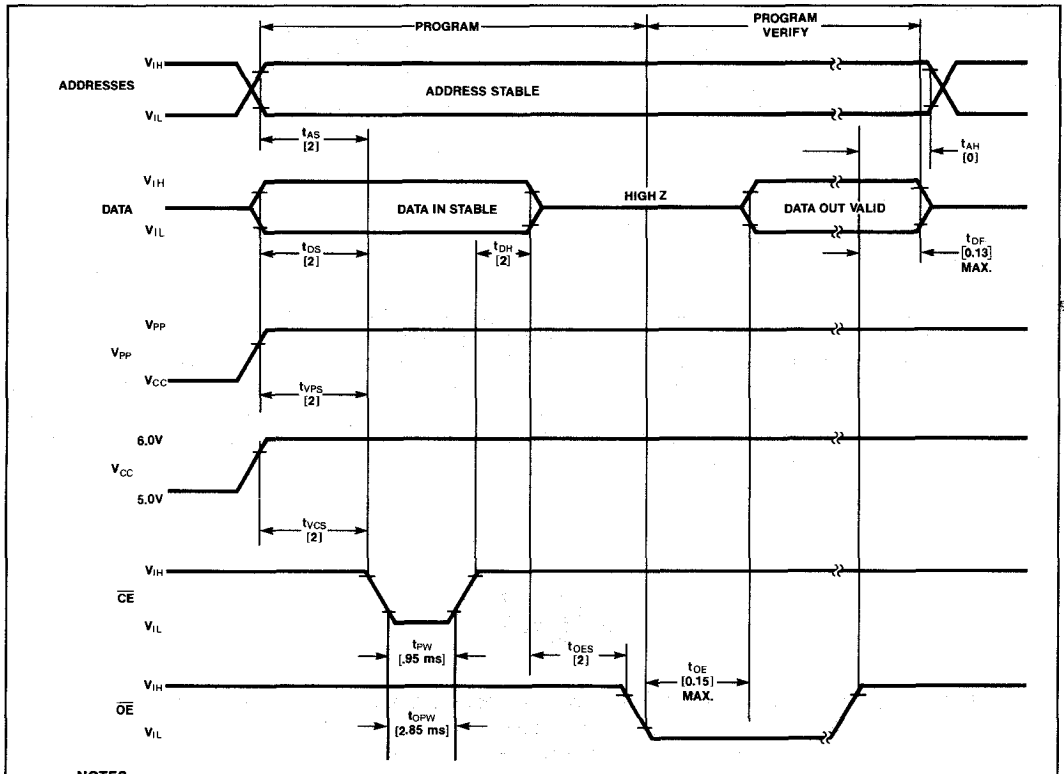


Figure 2. int$_e$ligent Programming™ Algorithm

27256 PROGRAMMING WAVEFORMS

With the replacement of the $\overline{PGM}$ signal by A14 on Pin 27, changes are required in the manner in which the 27256 is programmed. Figure 3 shows the waveforms required to program the 27256. As illustrated, the 27256 will be placed in the program mode when V_{PP} is set to 12.5 volts, and $\overline{CE}$ is pulsed to V_{IL}. The verify operation will then be selected with $\overline{CE}$ at V_{IH}, and $\overline{OE}$ held at V_{IL}. This results from multiplexing both the chip enable function and the programming enable function onto Pin 20. The V_{PP} level, either 5 volts or 12.5 volts, gates which function is selected. Table 1 indicates the various modes of operation of a 27256.

In on-board gang programming applications, care must be taken not to enable the outputs of all resident 27256 devices while in the verify mode. A common $\overline{OE}$ signal could cause bus contention. AR-294 will discuss this issue in detail.



NOTES:
1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A V_{IL} AND 2V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMODATED BY THE PROGRAMMER.
4. WHEN PROGRAMMING THE 27256 A 0.1μF CAPACITOR IS REQUIRED ACROSS V_{PP} AND GROUND TO SUPRESS SPURIOUS VOLTAGE TRANSIENTS WHICH CAN DAMAGE THE DEVICE.

Figure 3. int$_e$ligent Programming™ Waveforms

Table 1. 27256 Operational Modes

MODE \ PINS	CE (20)	OE (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
int$_e$ligent Programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
int$_e$ligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code

NOTES:
1. X can be V_{IH} or V_{IL}
2. V_H = 12.0V ± 0.5V

SUMMARY

The introduction of the 27256 continues Intel's leadership in high density EPROM storage capability. With this density increase comes the ability to design in system firmware, creating a more reliable, user-friendly environment for the computer operator. The int$_e$ligent Programming Algorithm developed for Intel's 2764 and 27128 EPROMs, provides many benefits, including lower costs, which result from higher system manufacturing throughput. In line with this strategy, the 27256 int$_e$ligent Programming Algorithm was designed to meet the technology requirements of the new device. With this algorithm, the 27256 may be programmed according to the waveforms shown in figure 3, ensuring programming reliability and efficiency.

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 987-8080.
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